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December 9, 2003

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Re: Applicant(s): Jason Cheng; Cyrus Tsui; Satwant Singh; Albert Chan; Ju Shen; Clement Lee
Assignee: Lattice Semiconductor Corporation
Title: Programmable Logic Device With Enhanced Wide Input Product Term Cascading
Serial No.: 10/619,711 Filed: 07/14/2003
Examiner: Unknown Group Art Unit: 2651
Docket No.: M-9559-2P US

Dear Sir:

Transmitted herewith are the following documents in the above-identified application:

- (1) Return-receipt postcard;
- (2) This Transmittal Letter (in duplicate);
- (3) Response to Notice to File Missing Parts of Nonprovisional Application;
- (4) A copy of the Notice to File Missing Parts of Nonprovisional Application;
- (5) Executed Declaration and Power of Attorney form;
- (6) Information Disclosure Statement;
- (7) PTO-1449 with copies of twelve (12) cited references; and
- (8) Submission of Formal Drawings with fifteen (15) sheets of formal drawings including Figures 1, 2A-1, 2A, 2A-2, 2A-3, 2A-4, 3, 4, 5A, 5B, 6, 7, 8, 9, 10, and 11.



No additional fee is required.

The fee has been calculated as shown below:

CLAIMS AS AMENDED

Claims Remaining <u>After</u> <u>Amendment</u>		Highest No. Previously <u>Paid</u> <u>For</u>		Present <u>Extra</u>	<u>Rate</u>	Additional <u>Fee</u>
Total Claims	Minus	20	=	x	\$18.00	\$
Independent Claims	Minus	3	=	x	\$86.00	\$
<input type="checkbox"/> Fee of _____ for the first filing of one or more multiple dependent claims per application						\$
<input checked="" type="checkbox"/> Fee for Late Oath Surcharge.						\$ 130.00
Total additional fee for this Amendment:						\$
<input checked="" type="checkbox"/> Conditional Petition for Extension of Time: If an extension of time is required for timely filing of the enclosed document(s) after all papers filed with this transmittal have been considered, an extension of time is hereby requested.						
<input type="checkbox"/> Please charge our Deposit Account No. 50-2257 in the amount of						\$
<input checked="" type="checkbox"/> Also, charge any additional fees required and credit any overpayment to our Deposit Account No. 50-2257						

Total: \$ **130.00**

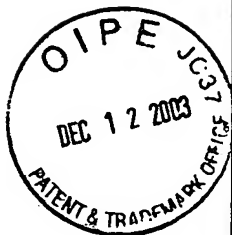
I hereby certify that this correspondence is being mailed via first class postage to the Commissioner for Patents, Alexandria, VA 22313-1450, on December 9, 2003.

Eric Hoover

December 9, 2003
Date of Signature

Respectfully submitted,

Jon W. Hallman
Attorney for Applicants
Reg. No. 42,622



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Jason Cheng; Cyrus Tsui; Satwant Singh; Albert Chan; Ju Shen;
Clement Lee
Assignee: Lattice Semiconductor Corporation
Title: Programmable Logic Device With Enhanced Wide Input Product Term
Cascading
Serial No.: 10/619,711 Filing Date: 07/14/2003
Examiner: Unknown Group Art Unit: 2651
Docket No.: M-9559-2P US

Irvine, California
December 9, 2003

Attn: Official Draftsperson
COMMISSIONER FOR PATENTS
Alexandria, VA 22313-1450

SUBMISSION OF FORMAL DRAWINGS

Dear Sir:

Applicants submit fifteen (15) sheets of formal drawings, consisting of Figures 1, 2A-1, 2A, 2A-2, 2A-3, 2A-4, 3, 4, 5A, 5B, 6, 7, 8, 9, 10, and 11, in the above-named application. If there are any questions regarding these drawings, please call the undersigned at (949) 752-7040.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 9, 2003.

Eric Hoover

12/9/03

Date of Signature

Respectfully submitted,

Jon W. Hallman
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Reg. No. 42,622

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